Segmented Dual-Gate MESFET's for Variable Gain and Power Amplifiers in GaAs MMIC

KEITH H. SNOW, MEMBER, IEEE, JAMES J. KOMIAK, AND DAVID A. BATES, MEMBER, IEEE

Abstract—**The design and performance of *C*-, *X*-, and K_u-band GaAs MMIC variable gain and variable power amplifier circuits using an improved segmented dual-gate MESFET device with binary scaled gate width ratios are reported. The demonstrated 35 dB control range, flat octave band gain response, and small incidental phase variation are significantly superior to conventional analog controlled devices. First pass performance of these digitally controlled circuits demonstrates the maturation of MMIC technology.**

I. Introduction

FUTURE AEROSPACE systems, such as multifunction active phased array radar and wide-band communication systems, require precise amplitude control to achieve the improved transmit/receive sidelobe levels the modern electromagnetic environment demands. Digitally controlled programmability imposes additional constraints that have evolved from adaptive pattern control requirements. The objective of this work was to develop variable gain amplifier (VGA) and variable power amplifier (VPA) circuits using dual-gate MESFET's to provide transmit/receive architectures with precise amplitude quantization over a 30 to 40 dB control range while minimizing insertion phase variations, and thus calibration complexity, incurred by gain state switching. Additional objectives were wide bandwidth (to allow generic application) and compactness, factors leading to low-cost, high-yield fabrication.

II. MESFET Device

Building on the results of Hwang *et al.* [1], the amplifier circuits developed at GE use segmented dual-gate MESFET's (SDGFET's) to obtain precise gain control. In this approach, the second gate of the dual-gate MESFET is digitally controlled to switch on and off portions of the SDGFET total gate periphery to achieve a desired gain state. The on/off control is created by switching the gate #2 bias voltage levels between saturation and pinch-off, making the device CMOS compatible, while the gate #1 voltage is held constant. When the reference maximum gain state of the SDGFET is chosen so that all segments of the device are biased on, a specific gain/attenuation level can be selected by turning off portions of the total SDGFET periphery. If the segments are scaled in a binary fashion, a linear gain/attenuation curve results with 6 dB steps between most significant bit (MSB) states. From a pattern control viewpoint, this scale is desirable, since it provides finer weight control of center elements and faster peripheral roll-off of typical weighting functions.

Harris Microwave Semiconductor selectively implanted 0.5 μm gate length devices were used as the basis for the designs. These planar devices, fabricated on low-pressure LEC material, employ a dual-level plating scheme to achieve a large-cross-section, low-resistance plated T-shaped gate as well as a source air bridge interconnection. De-embedded small-signal *S*-parameters of a 200 μm periphery dual-gate device were measured from 0.5 to 20 GHz with the second gate short-circuited to ground and a voltage beyond pinch-off applied. Equivalent circuits, including fixturing and gate #2 termination parasitics for both the on and the off state, were then fitted to the data.

Fig. 1 depicts the monolithic dual-gate circuit model used for small-signal circuit design, with element values given for both states at the bias point of 4 V and 20 percent of I_{dss}. Unlike the dual-gate model used in [1], this improved model consists of two single-gate FET devices in series, augmented with gate #1 to gate #2 and gate #1 to drain capacitances. Note that it is difficult to model a dual-gate GaAs MESFET because of its complicated geometry and the effect of the terminal impedance at gate #2. Therefore, extreme care in fixturing, de-embedding, and modeling is required since this base model will be scaled up and down in periphery to obtain the SDGFET model as a function of gain/attenuation state.

III. Circuit Design

To obtain the small-signal models required for circuit design, on and off state models were generated for the MSB segments via binary scaling of the Fig. 1 models. By paralleling the segment models, the MSB state models were generated. For the VGA designs, several factors influenced the size of the segments, including power consumption, circuit size, and dynamic range requirements. Six bits were required in the ratio of 1–2–4–8–16–32 for which several SDGFET device layout geometries were constructed. Photomicrographs of three possible device geometries used successfully in variable gain amplifier circuits (labeled devices A, B, and C) are shown in Fig. 2.

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The authors are with the GE Electronics Laboratory, Syracuse, NY 13221.

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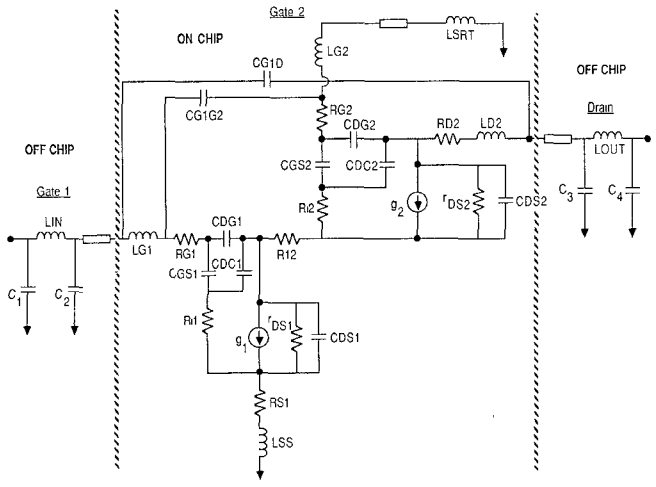


Fig. 1. Monolithic model of 0.5 μm × 200 μm dual-gate MESFET device (on/off).

As amplifiers, all three SDGFET devices are operated in a cascode configuration providing six-bit gain control, with the second gate RF grounded via a shunt capacitor, and use resistors for isolation from the control voltage source. The relative phase shift of the VGA between states can be minimized by proper selection of the gate #2 termination capacitors. These capacitors are scaled in proportion to the gate width of the particular segment being terminated.

The construction of the four MSB's is similar for all three devices: each utilizes 200, 100, 50, and 25 μm gate width segments. For devices A and B, the last two bits were obtained using a resistive divider and 50/25 μm segments to avoid fringing effects that typically perturb scaling rules when small peripheries are required. In addition, the geometrical layouts of devices A and B are different with respect to the orientation of the segments and their proximity to the via-hole source grounding. As the photomicrograph shows, the symmetrical layout of device B eliminates the long gate #2 control lines and large drain manifold areas seen in device A, where there is no active device material and hence unknown device parasitics. In device C, the two least significant bit (LSB) gate segments are scaled directly to the proper ratios. These 12.5/6.25 μm gate #2 segments share gate #1 with the 50/25 μm segments, respectively, providing for a more compact layout.

The variable power amplifier (VPA) required three bits of control per stage; consequently, 800, 400, and 200 μm segments were selected. To prevent self-bias under power conditions, the gate #2 isolation resistors were reduced to values that allowed the control voltage to source/sink the mA of current required. In addition to operation at the power bias point of 8 V and 60 percent of I_{dss}, the variable power amplifier required a class A power amplifier design technique. Large-signal circuit design utilized a modified version of the methodology described in [2] for single-gate devices with the drain conductance substitution applied to both devices in the cascode connection. Similarly, the design philosophy employed small-signal interstage design augmented by large-signal interstage load-pull analysis and an off-chip output matching on a high-dielectric-constant (ϵ_r = 37) substrate. The result is maximized power/efficiency, a reduced chip size increasing wafer yield and reducing chip cost, and an overall amplifier envelope commensurate with a totally monolithic implementation.

IV. MMIC Fabrication

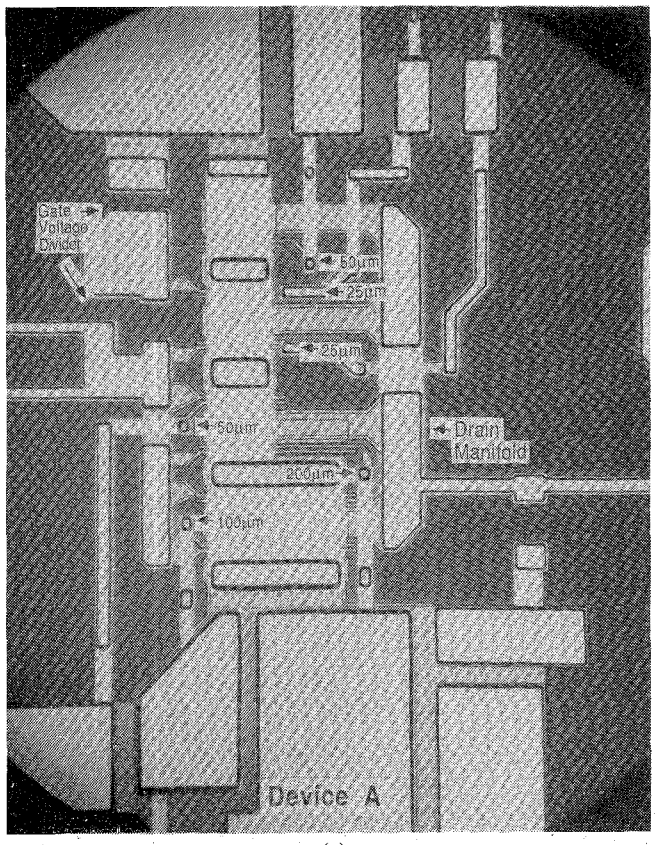
Harris Microwave Semiconductor fabricated the designs using its standard MMIC process. Selective ion implantation was employed, and the N and N^+ implants that form the MESFET structure were also used for high and low sheet resistance resistors. After the formation of ohmic contacts and Schottky barrier gates, the large-cross-section plated gate was formed, with this layer additionally functioning as the first level metal interconnect for transmission lines and capacitor bottom plates. A silicon nitride dielectric used for the MIM capacitors was deposited next, followed by the second level of plated metal. The second level plating forms air bridge interconnects, capacitor top plates, and increased cross section transmission lines (used in conjunction with first metal). The substrate was thinned, the via holes etched, the backside metallized, and the wafer scribed and separated into individual MMIC's.

V. Small-Signal Amplifier Performance

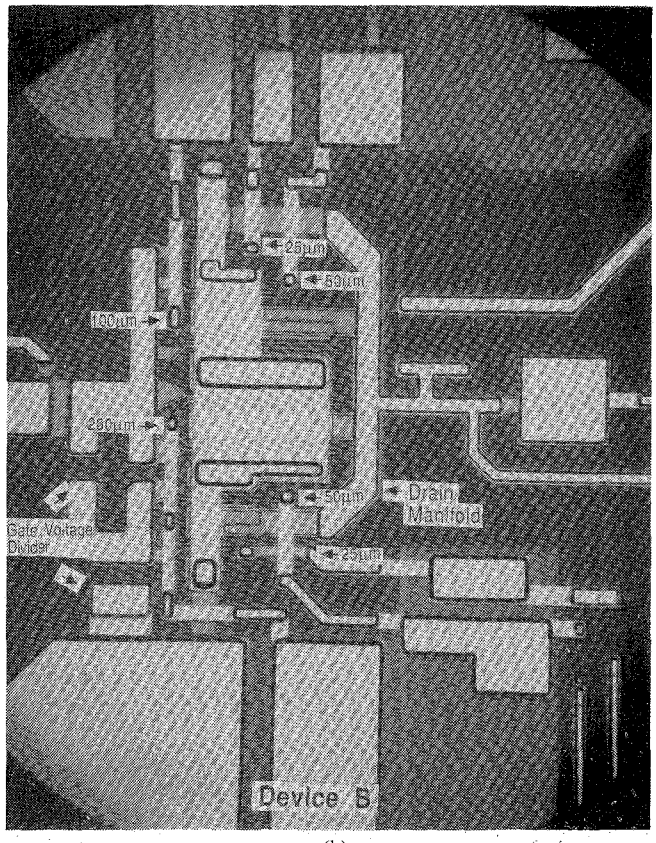
The *C*-/*X*-band variable gain amplifier (CXVGA) shown in Fig. 3 consists of a six-bit SDGFET with integral bias and matching circuits. Chip size is 1.44 mm × 1.5 mm. Small-signal gain is 5.5 dB ± 0.5 dB from 5.5 to 10.5 GHz with better than a 35 dB range (Fig. 4). Measured input and output return losses were 6 to 12 dB from 5 to 11 GHz, with less than 3 dB maximum variation across all 64 gain/attenuation states.

The precise control achieved is demonstrated in Fig. 5, where the normalized amplitude performance is plotted for all 64 states from 4 to 11 GHz. Across this band, linearity error is better than 2.5 percent. Incidental phase variation with state is less than 6° over a 20 dB control range, as shown in Fig. 6.

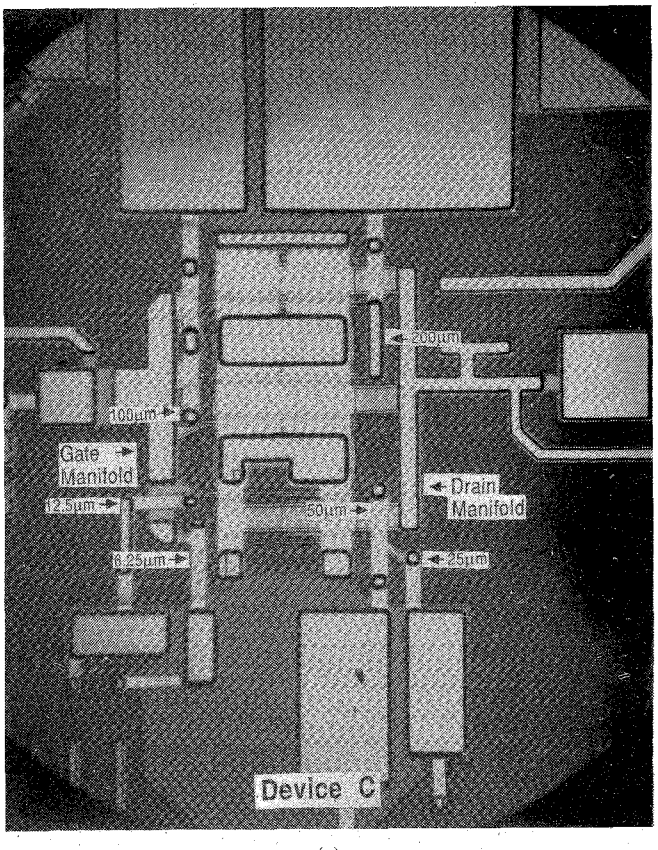
The *X*-/*Ku*-band variable gain amplifier (Fig. 7) shows similar performance, exhibiting a small-signal gain of 1.5 dB ± 0.5 dB over greater than octave bandwidth from 6.4 to 15.6 GHz, as shown in Fig. 8. The incidental phase shift of this circuit from 6 to 18 GHz is less than 10° over a 20 dB control range. Chip size is 1.02 mm × 1.19 mm.



(a)



(b)



(c)

Fig. 2. Segmented dual-gate MESFET device constructions. (a) Asymetrical and (b) symetrical layouts with voltage divider for LSB's. (c) LSB's scaled directly to 12.5 μm and 6.25 μm gate widths.

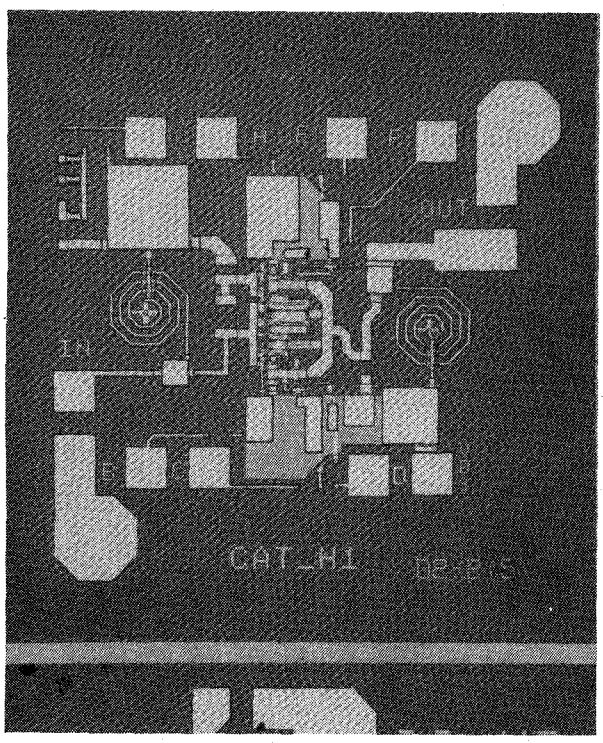


Fig. 3. Photograph of the *C*-/*X*-band variable gain amplifier (CXVGA).

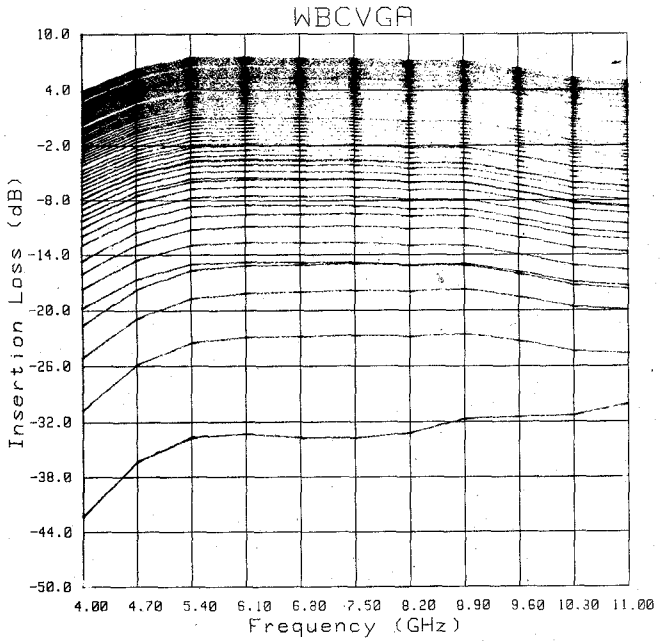


Fig. 4. CXVGA gain/attenuation versus state.

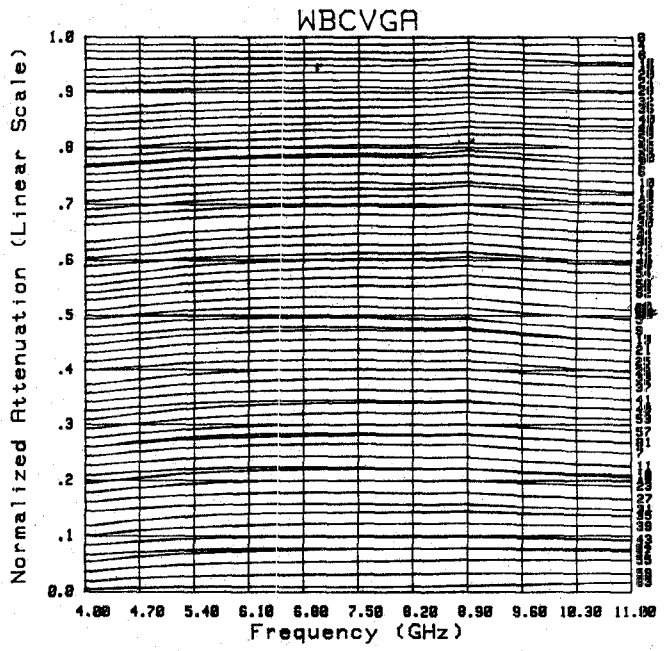


Fig. 5. CXVGA linear scale amplitude across 64 states.

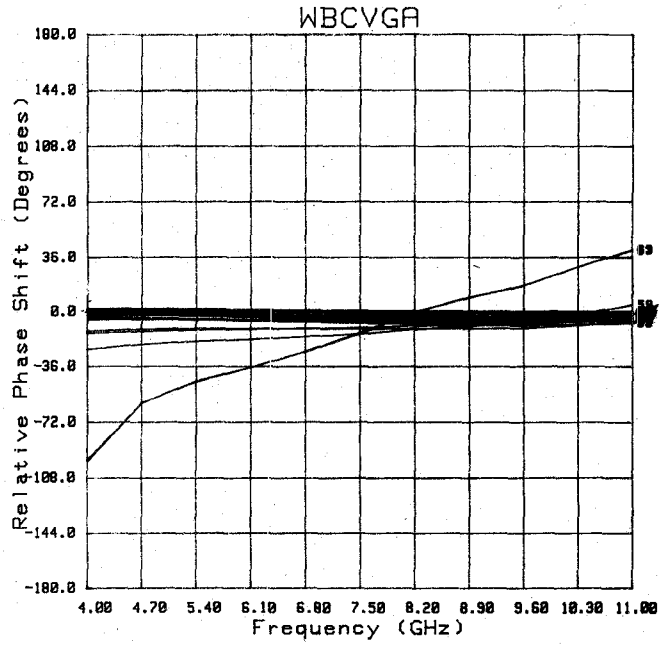


Fig. 6. CXVGA incidental phase shift across 64 states.

VI. Power Amplifier Performance

The *X*-band variable power amplifier (XVPA) shown in Fig. 9 is a two-stage design consisting of a 1.4 mm segmented dual-gate device of 100 μm unit finger width that drives a pair of 1.4 mm devices. Gate resistors and an odd-mode stabilization resistor provide immunity to external bias connections and enhance low-frequency stability (this MMIC is unconditionally stable both in and out of band). An additional resistor in the interstage dampens the Q of this network and desensitizes the interstage match to typical device variations.

The gate and drain bias networks are integral to the design acting as impedance matching elements. Chip size is 3.57 mm $\times$ 2.5 mm. The off-chip output matching network measures 1.7 mm $\times$ 2.1 mm. Small-signal gain is 14.5 dB $\pm$ 1.5 dB (maximum) from 7.0 to 11.5 GHz and is controllable over a 35 dB control range, as shown in Fig. 10. The circuit exhibits minimal phase variation, with less than 10° incidental phase shift over a 20 dB dynamic range and less than 15° over a 35 dB dynamic range (Fig. 11). The XVPA demonstrates digitally controlled linear

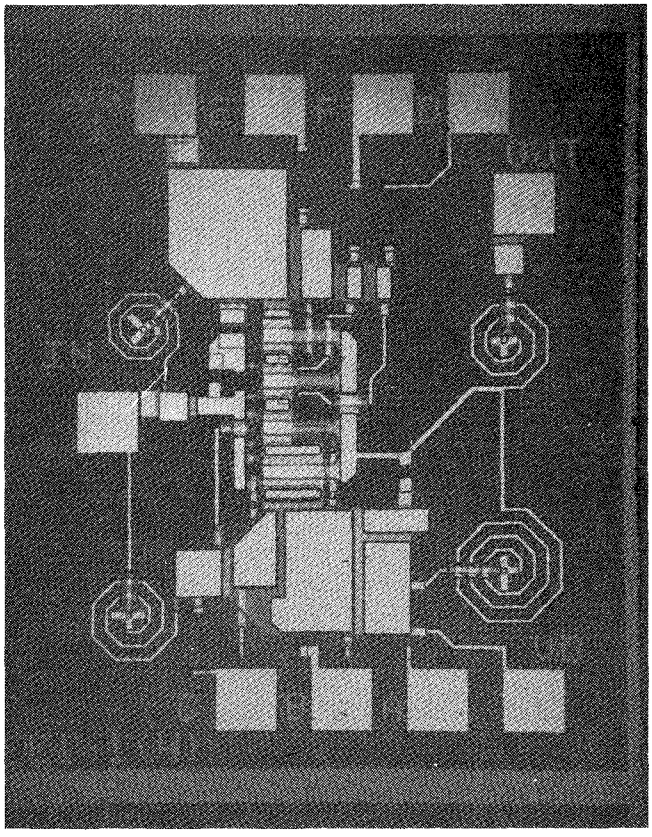


Fig. 7. Photograph of the *X*-/*Ku*-band variable gain amplifier.

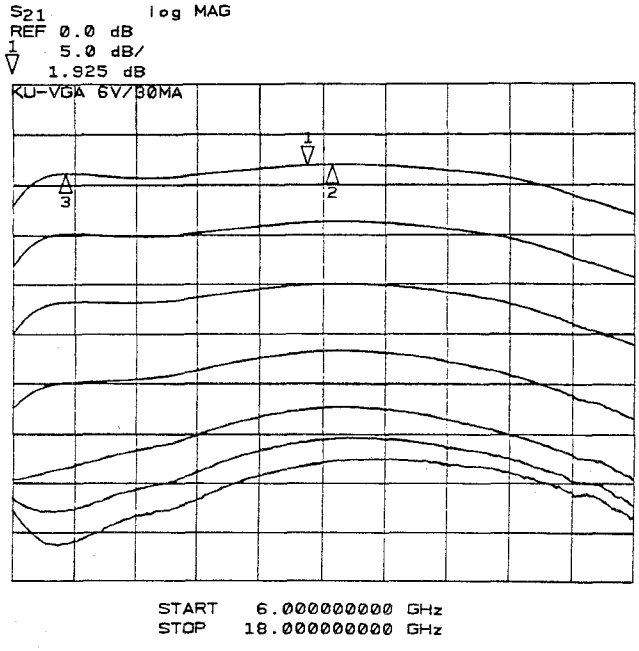


Fig. 8. *X*-/*Ku*-band VGA gain/attenuation at MSB states.

transmit tapering from 0.5 W peak with 10–15 percent power-added efficiency over the first 10 dB of dynamic range. The XVPA degradation in efficiency is much less than the more conventional approach, where a saturated power amplifier is operated in the linear region. Fig. 12 depicts the output power for selected states, and Fig. 13 depicts the normalized efficiency versus output power.

VII. Digital Versus Analog Control

For array applications, digital control is desired. Both amplitude and phase, as a function of amplitude state, are important since array elements must track in amplitude and phase irrespective of amplitude weighting. Poor tracking necessitates more complex calibration and control algorithms or lookup tables, and may limit signal in-

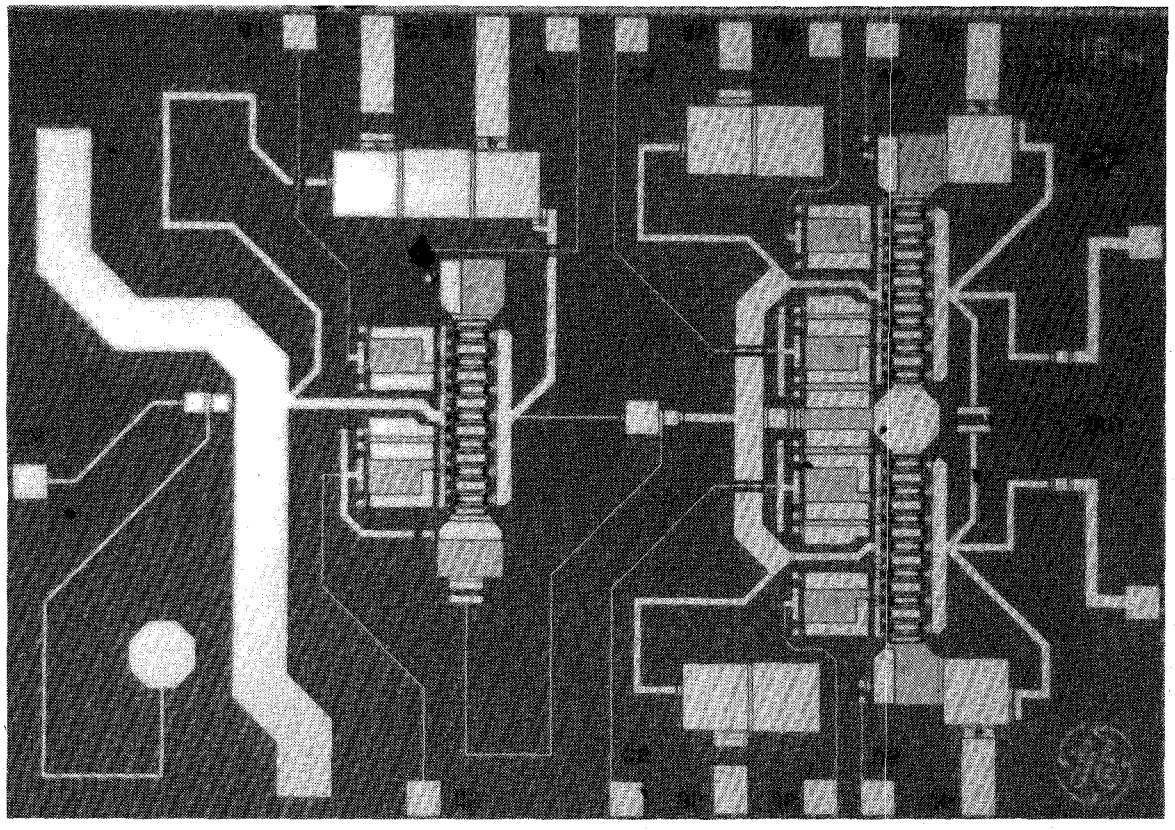


Fig. 9. Photograph of the *X*-band variable power amplifier (XVPA).

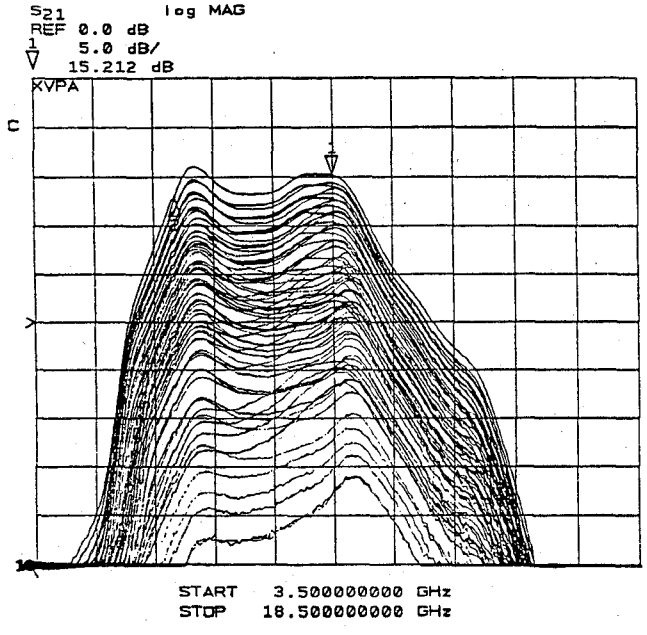


Fig. 10. XVPA gain/attenuation across 64 states.

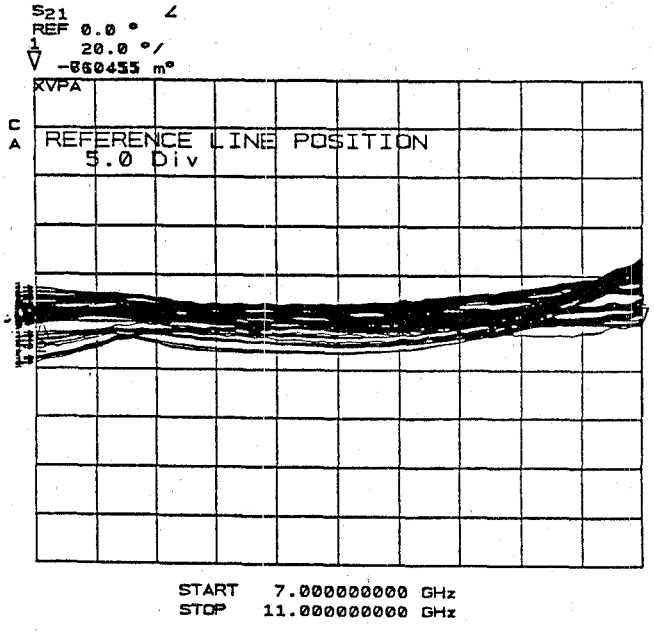


Fig. 11. XVPA incidental phase shift across 64 states.

stantaneous bandwidth. Variable gain amplifier performance was evaluated using analog and digital control on the gate #2 segments. The family of curves in each of these plots depicts the relative amplitude (Fig. 14(a) and (b)) and phase characteristics (Fig. 14(c) and (d)) at 11 frequencies from 6 to 12 GHz. The resulting amplitude characteristics for digital and analog control are as expected: digital control provides considerably better linearity. The resulting phase characteristics also demonstrate a substantial advantage for the digitally controlled circuit. Over the range from maximum gain to 20 dB attenuation, the analog controlled circuit exhibits 60° phase shift. On the other hand, the digitally controlled circuit exhibits only 3° phase shift.

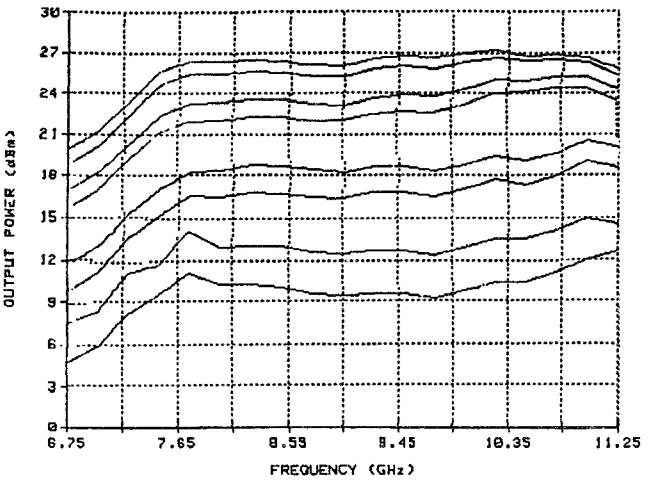


Fig. 12. XVPA output power at selected states

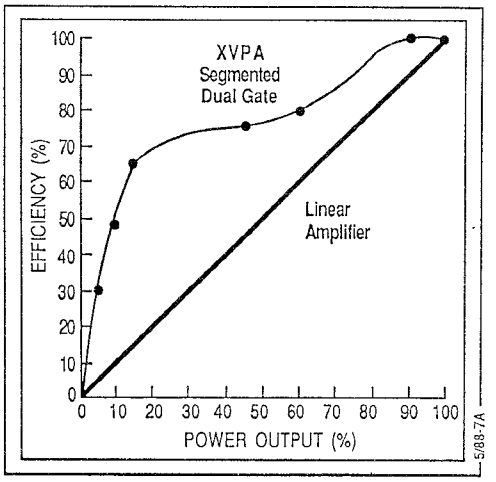


Fig 13 XVPA normalized efficiency versus output power.

In the digitally controlled circuit, phase variation can be minimized by proper selection of the gate #2 RF terminations, since the periphery is switched between only two states: saturation and pinch-off.

The digitally controlled circuits also demonstrate remarkable repeatability from device to device. Fig. 15 illustrates (a) analog and (b) digital amplitude variation for six circuits from different wafers measured at 9 GHz. The variation in amplitude between digitally controlled units was 3 percent, while the variation using analog control was 15 percent. The relative phase tracking between units (Fig. 15(c) and (d)) is as high as 40° for analog control and typically less than 4° for digital control. These results demonstrate that sophisticated and individually adjusted control circuitry, characteristic of analog circuits, is not required for circuits operated digitally.

VIII. Applications

This family of variable gain amplifiers has been developed for MMIC active phased arrays. Excellent design flexibility in performance parameters results in a wide range of applications. For receive applications, the six-bit digital control in linear voltage steps provides 0.14 dB amplitude resolution, which supports precise digital array calibration, temperature compensation, and amplitude taper with isotropic error sidelobes of −41 dBi (considerably smaller than typical design sidelobe levels). These circuits operate on the underlying circuit principle that gain is proportional to g_m^2. Therefore, circuit relative gain and phase characteristics are periphery ratio dependent, allowing flexibility in the choice of dc operating point. As a result, a design can be optimized for low noise, low dc power, or high output power applications through proper bias point selection and/or periphery scaling. Circuit designs have demonstrated power consumption of less than 50 mW, noise figures of less than 5.5 dB, and power output capability of 0.5 W at X-band.

In applications such as array transmitters, where amplitude taper may be desired, efficiency of attenuated elements is a prime consideration. This circuit approach is superior to linear amplifiers for maintaining high effi-

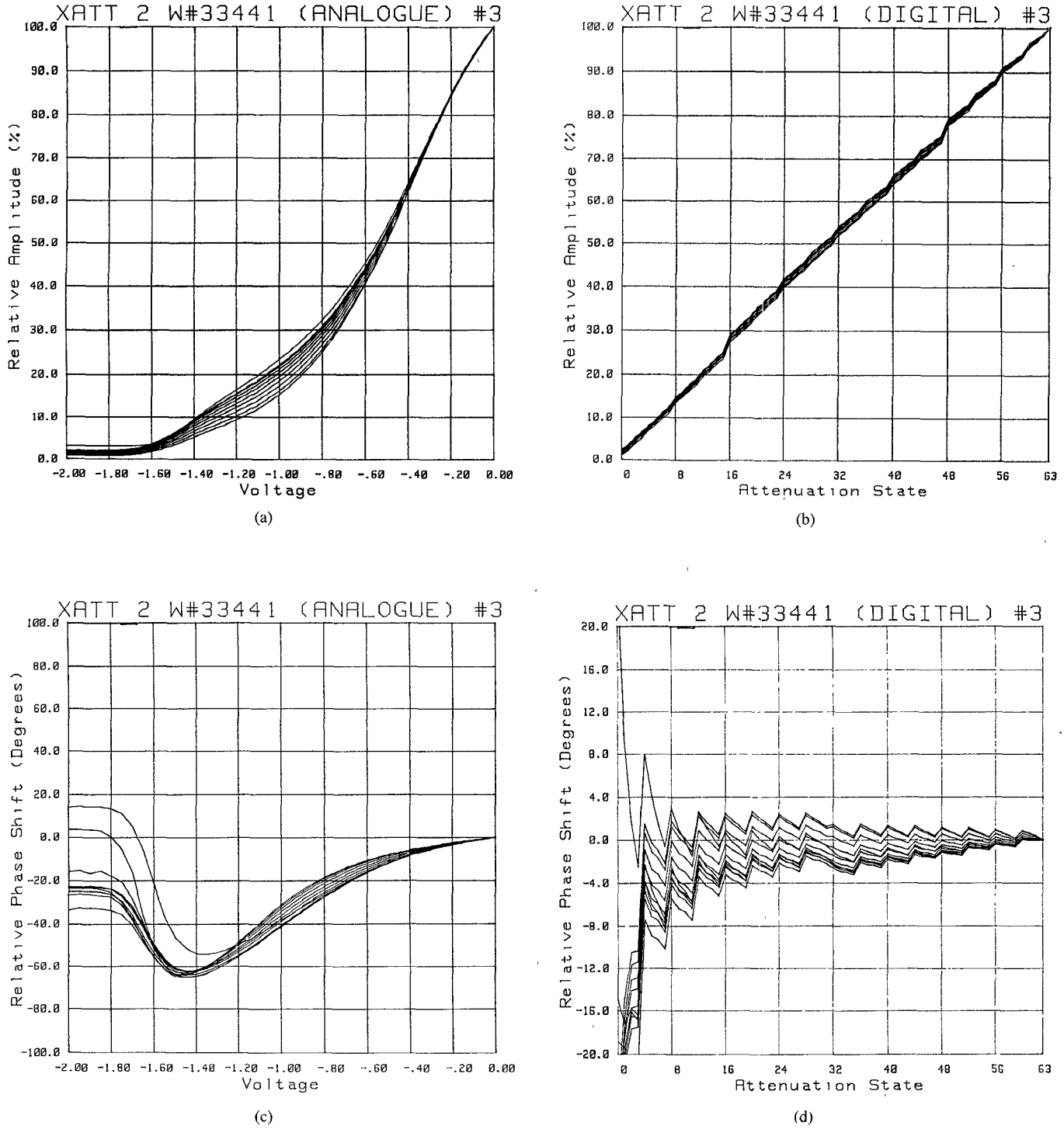


Fig. 14. Amplitude and phase variation with frequency: 11 frequencies measured from 6 to 12 GHz. (a) Amplitude versus analog control (b) Amplitude versus digital control. (c) Phase versus analog control (d) Phase versus digital control.

ciency at reduced power levels (Fig. 13) since "on" state gate periphery can be operated at the bias point that maximizes efficiency.

In future active arrays, it is anticipated that digital beamsteering computation and control will be exploited for their inherent advantages in cost, size, speed, and noise immunity. As a result, digitally controlled microwave circuits will be much more desirable than their analog counterparts.

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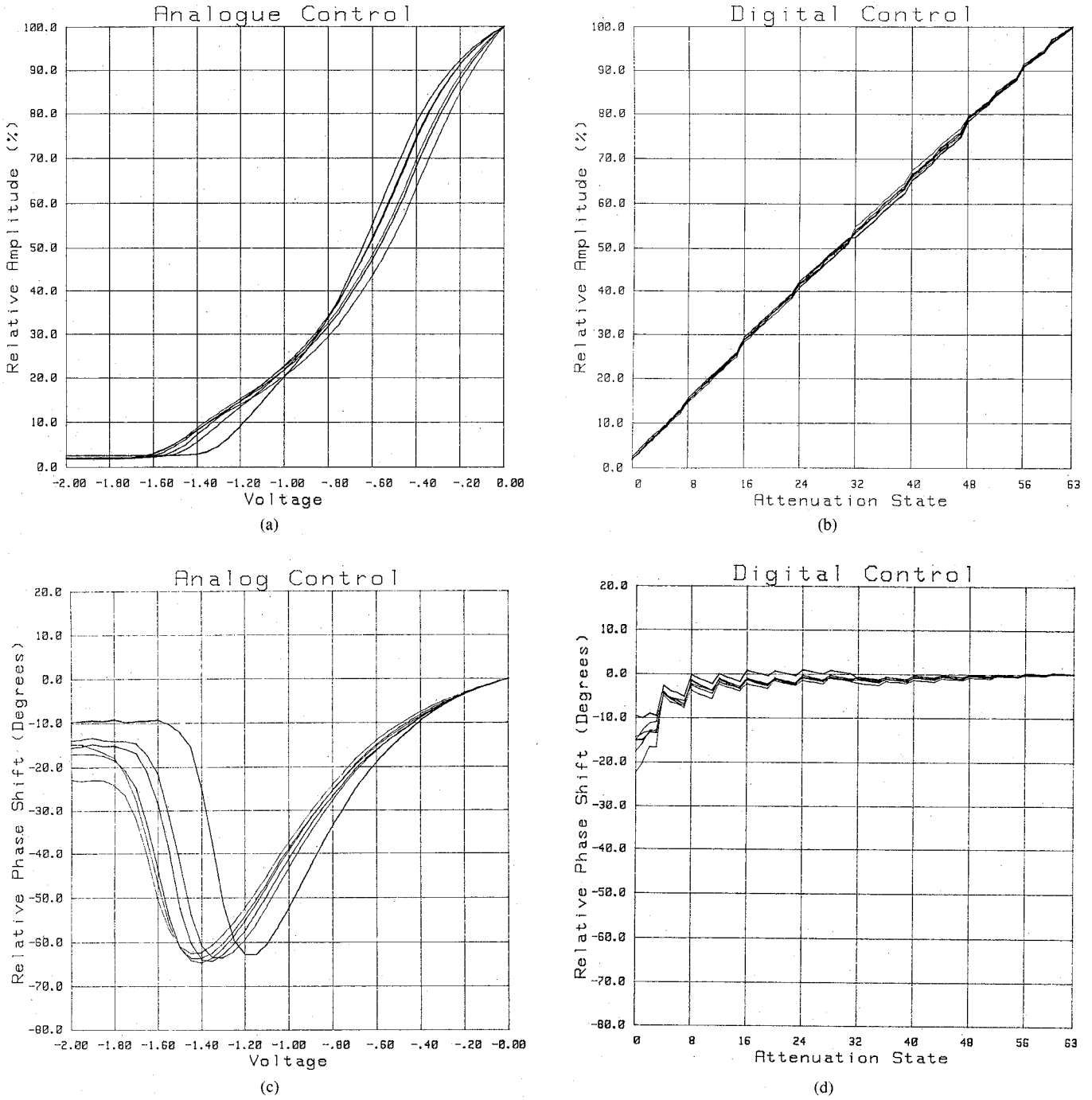

Fig. 15. Amplitude and phase variation by device: device data for six devices measured at 9 GHz. (a) Amplitude versus analog control. (b) Amplitude versus digital control. (c) Phase versus analog control. (d) Phase versus digital control.

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REFERENCES

[1] Y. C. Hwang, D. Temme, Y. K. Chen, and R. J. Naster, "A microwave phase and gain controller with segmented dual gate MESFET's in GaAs MMIC," in *Dig. 1984 IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp.*, May 1984, pp. 1–5.

[2] J. J. Komiak, "Wideband $C/X/K_u$-band power MMIC's," in *Dig. 1987 IEEE GaAs IC Symp.*, Oct. 1987, pp. 215–218.

Keith H. Snow (S'84–M'87) was born in Northampton, MA, on February 14, 1960. He received the B.S. and M.S. degrees in electrical and computer engineering from the University of Massachusetts, Amherst, in 1985 and 1987, respectively.

After completing his undergraduate studies, Mr. Snow joined the GE Electronics Laboratory, Syracuse, NY, where he designed and evaluated *Ka*-band microstrip patch radiating elements. Later in 1985, he entered the University of Massachusetts Microwave Engineering Program. Returning to GE in 1986, Mr. Snow worked on theoretical analyses of the electromagnetic fields in phased

array antenna radiating elements. Since 1987 he has been involved with the development of GaAs MMIC's for a variety of communication and phased array radar systems. More recently, he has been involved with the design of HEMT low-noise amplifiers for applications at millimeter-wave frequencies. He is currently responsible for microwave technology program development.

Mr. Snow is a member of Eta Kappa Nu and is Chapter Chairman of the Antennas & Propagation and Microwave Theory & Techniques Societies in Syracuse, NY.

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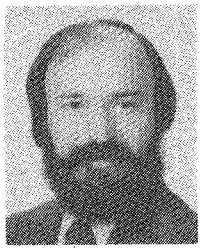

James J. Komiak was born in Chicago, IL, on October 16, 1953. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Cornell University, Ithaca, NY, in 1974, 1976, and 1978, respectively. His Ph.D. research was directed towards a novel broad-band matching technique for arbitrary loads utilizing measured data directly.

In 1983, he joined the GE Electronics Laboratory in Syracuse, NY, where he is presently Principal Staff—Microwave/Millimeter-Wave Technology. Previously, between 1978 and 1983, he was with IBM Federal Systems Division in Owego, NY, where he was responsible for ESM/ELINT antenna and receiver development. While there he designed several hybrid RF/microwave and analog/digital pages that are still in production for a variety of mil-spec applications. His current activities include MMIC and hybrid MIC circuit and T/R module designs for radar, ECM, shared aperture, and communication system applications. Dr. Komiak has designed and consulted on several broad-band multistage temperature compensated *Ku*-band MIC amplifiers with limiting, low noise, power, and gain-tracking specifications that are now in production as part of the ALQ-161 for the B-1B. State of the art MMIC's that he has designed include a 1 dB noise figure L-band LNA, 8 W S-band HPA's, 1.3 W and 2 W *X*-band HPA's, a 0.5 W 6 to 18 GHz HPA, a 1 W linear *Ku*-band HPA, a 0.5 W segmented dual gate *X*-band variable power amplifier, and a two-stage *V*-band LNA using HEMT technology.

Dr. Komiak is a member of the Association of Old Crows and has numerous publications relating to circuit theory, GaAs MMIC devices and technology, solid state apertures, and RF/microwave design.

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David A. Bates (S'77–M'77) received the B.S. degree in electrical engineering in 1977 from the University of Michigan, Ann Arbor.

He joined the Phased Array Technology section of the GE Electronics Laboratory, Syracuse, tory, Syracuse, NY, in 1985. He is involved in the design of MMIC's and both microwave and millimeter-wave modules and arrays, with applications in phased array communications and radar systems spanning frequencies from *L*-band to *V*-band. Mr. Bates is a project leader in the design of monolithic arrays and architectures, and is currently working on MMIC modules and the development of advanced packaging and interconnect technologies. He has developed millimeter-wave fixtures and transitions and a state-of-the-art millimeter-wave noise measurement system. Prior to joining GE, he was with Harris Government Aerospace Systems Division in Melbourne, FL, where he was involved in the design of state-of-the-art hybrid microwave integrated circuits and subsystems for adaptive phased arrays, frequency synthesizers, and signal processing.